REMARKS

Claims 59-83 are pending in the application. Claims 60-63 and 66-71 have been amended. Claims 60-64 and 66-70 are objected to for a dependency error. Claims 65 and 77-83 are allowed. Claims 73-76 are objected to for being dependent upon a rejected claim, but are otherwise allowable.

Claims 60-64 and 66-70 stand objected to for a dependency error. The Examiner notes that claims 60-64 are all dependent upon claim 60. The Examiner is correct in determining that claims 60-64 actually depend upon claim 59. Similarly, claims 66-70 are all dependent upon claim 66. The Examiner is correct in determining that claims 66-70 actually depend upon claim 65. Claims 60-64 and 66-70 have been accordingly modified, and Applicant respectfully requests that the objection be withdrawn.

Claims 59-64, 71 and 72 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Collins. Because Collins does not disclose each element of claims 59-64, 71 and 72, Applicant respectfully requests that the rejection be withdrawn.

Claim 59 discloses a method of generating a latency drift signal. The method includes, inter alia, "generating a first signal for indicating that data requested has been received; generating a plurality of derivative signals from said first signal, said plurality of derivative signals corresponding to a plurality of states of said first signal at a respective plurality of times; [and] comparing at least two of said derivative signals." A latency drift signal is generated when the compared "at least two of said derivative signals exhibit a predetermined relationship." Collins does not disclose these elements and therefore does not anticipate claim 59.

Collins relates to a method for "effectively determining the sensitivity of logic systems to timing variations." Collins, col. 3, lines 17-20. Accordingly, the timing of clock signals transmitted via a clock distribution network is incrementally adjusted to similarly adjust the response window for various logic components. Collins, col. 3, lines 29-37; col. 8, lines 6-42. Data errors and component failures may result by adjusting the response window, thus determining the timing sensitivity of various components and overall logic systems. *Id.*

However, Collins does not disclose "generating a first signal for indicating that data requested has been received," as recited in claim 59. Collins describes a typical logic path data transfer, wherein data is transferred between a sending and a receiving shift register latch. Collins, col. 4, lines 64-68; col. 5, lines 1-4. But Collins is silent as to the types of data or non-data signals transmitted on the logic path. Specifically, Collins does not refer to the generating of a unique signal indicating that a data request has been received. Collins refers only generally to data signals. Collins, col. 5, lines 1-20.

Additionally, Collins does not disclose "generating a plurality of derivative signals from said first signal, said plurality of derivative signals corresponding to a plurality of states of said first signal at a respective plurality of times," as recited by claim 59. Clearly, if Collins does not disclose the generating of a first signal, it is impossible to generate "a plurality of derivative signals from said first signal." Instead, Collins teaches the generation of various delayed timing signals derived from a master clock. Collins, FIGS. 11A-D; col. 10, lines 42-54. A user selects a desired set of delayed timing signals to be applied, and then runs the logic circuit using the delayed timing signals in order to monitor the number of logic path errors that occur. Collins, col. 10, lines 17-26. The various timing signals of Collins are different from the "plurality of derivative signals from said first signal" of claim 59. In claim 59, derivatives of the signal indicating that a data requested had been received are generated, not clock signal derivatives.

As recited by claim 59, at least two of the first signal derivatives are compared. Obviously, Collins failure to disclose both a first signal for indicating that data requested has been received and any derivatives of said first signal makes it impossible to compare any derivative signals. Applicant points out that the truth table of FIG. 10 of Collins relates to the various delayed clock signals, not a comparison of first signal derivatives.

Similarly, it is impossible to generate "a latency drift signal when said at least two of said derivative signals exhibit a predetermined relationship" if the necessary derivative signals are never derived. Collins fails to show any signal in response to a comparison of derived signals. Collins does generate error signals, but these are in response to errors caused by shifting

the timing of response windows in the logic path, and are not specifically in response to a comparison of signals derived from a first signal for indicating that data requested has been received.

Accordingly, because Collins fails to disclose every element of claim 59, Applicant submits that claim 59 is allowable and the rejection should be withdrawn. Claims 60-64 are each dependent upon claim 59, and thus incorporate all of the elements and limitations of claim 59. Hence, claims 60-64 are also allowable over Collins for at least the reasons stated above.

Claim 71 discloses a latency drift detector. The latency drift detector includes, inter alia, "means for receiving a ready signal of a programmable response time memory component whose response time is being measured; [and] means for generating a plurality of data outputs derived from said ready signal, said plurality of data outputs indicating a respective time within a response window from a plurality of clock signals." Because Collins fails to disclose each of the noted elements, it can not anticipate claim 71.

As stated above, Collins fails to disclose "a ready signal of a programmable response time memory component." Furthermore, Collins fails to disclose "means for generating a plurality of data outputs derived from said ready signal." Collins only discloses the derivation of various timing signals from a master clock signal and the use of the derived timing signals to test the sensitivity of various logic components. Collins, FIGS. 11A-D; col. 3, lines 29-37. Collins does not disclose means for deriving a plurality of data outputs from a ready signal of a programmable response time memory component. As such, claim 71 is allowable over Collins. Claim 72, which depends upon claim 71, and thus incorporates each of the elements and limitations of claim 71, is also allowable. Applicant respectfully requests that the rejection of claim 72 be withdrawn.

Claims 73-76 are objected to for being dependent upon claim 71, which stands rejected, but are otherwise allowable. However, as stated above, claim 71 is allowable over Collins. Thus, claims 73-76 are also allowable, and Applicant respectfully requests that the objection be withdrawn as to these claims.

In view of the above amendment, Applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

By _____

Thomas J. D'Amico
Registration No.: 28,371
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorney for Applicant